ABSTRACT

A method of electrically isolating and operating electro-optical components integrated in a monolithic semiconductor photonic chip, such as an EML or PIC chip. A bias, V_C, is applied to the isolation region so that any parasitical current path developed between adjacent active or passive optical components, now separated by an isolation region, is established through the electrical isolation region and clamped to the bias, V_C. The applied bias, V_C, may be a positive bias, a negative bias, or a zero or a ground bias. The electrical isolation regions are formed by spatial current blocking regions formed at adjacent sides of the electrical isolations region transverse to a direction of light propagation through the optical components, or between the electrical isolation regions and adjacent optical components. The spatial current blocking regions may be comprised of a pair of spatially disposed trenches or ion implanted regions or high resistance implanted regions.